Please read the following reference material for lectures delivered after mid-semester break:

Topic: Ratioed logic circuits and sizing

i. Chapter 9 section 9.2.2 from ‘CMOS VLSI Design’ by Neil H.E. Weste and David Harris.

ii. Chapter 6 section 6.2.2 from "Digital Integrated Circuits - A Design Perspective" by J. M. Rabaey.

Topic: CMOS logic circuits and method of logical effort

i. Chapter 9 section 9.2.1 from ‘CMOS VLSI Design’ by Neil H.E. Weste and David Harris, 4th edition, Addison-Wesley/Pearson.

ii. Chapter 6 section 6.2.1 from "Digital Integrated Circuits - A Design Perspective" by J. M. Rabaey.

Topic: Pass transistor and transmission gate logic

i. Chapter 7 section 7.5 and chapter 9 section 9.2 from ‘CMOS Digital Integrated Circuits’ by Sung-Mo (Steve) Kang and Yusuf Leblebici.

ii. Chapter 6 section 6.2.3 from "Digital Integrated Circuits - A Design Perspective" by J. M. Rabaey.

Topic: Dynamic circuit and sizing

i. Chapter 6 section 6.3.1 – 6.3.3 from "Digital Integrated Circuits - A Design Perspective" by J. M. Rabaey.

ii. Chapter 9 section 9.2.4.0 (not section 9.2.4.1) from ‘CMOS VLSI Design’ by Neil H.E. Weste and David Harris, 4th edition, Addison-Wesley/Pearson.

Topic: Sequential circuits, latches and flip-flops/registers, timing analysis

i. Chapter 7 section 7.1 – 7.3.1 from "Digital Integrated Circuits - A Design Perspective" by J. M. Rabaey.

ii. Chapter 10 section 10.1 (except 10.2.4) – 10.3.2 from ‘CMOS VLSI Design’ by Neil H.E. Weste and David Harris, 4th edition, Addison-Wesley/Pearson.

iii. (Optional) Chapter 8 from ‘CMOS Digital Integrated Circuits’ by Sung-Mo (Steve) Kang and Yusuf Leblebici.

Topic: Static and Dynamic RAM

i. Chapter 8 section 8.1. – 8.3 from "Microelectronics Circuit Design" by R. C. Jaeger and T. N. Blalock, 4th Edition. (Read only the 6-T SRAM and 1-T DRAM cells, T: transistor).

ii. (Optional) Chapter 10 from ‘CMOS Digital Integrated Circuits’ by Sung-Mo (Steve) Kang and Yusuf Leblebici.